Claims

What is claimed is:

1. A method of fabricating a p-n junction in an electronic device comprising:

forming a slot region for a doped polycrystalline semiconductor plug material within an outer periphery of an etched window region, said window region formed by etching a film stack residing on a topmost surface of a semiconductor substrate, said substrate having a first conductivity type;

filling said slot region with said polycrystalline semiconductor plug material;

depositing a dielectric separation layer over said polycrystalline semiconductor plug material and on an uppermost surface of said film stack;

implanting a dopant into an area of said substrate located within a region circumscribed by said slot region;

depositing a spacer over said dielectric separation layer;

etching said spacer and said dielectric separation layer anisotropically to form a dielectric boot shape on a lower edge of said dielectric separation layer, said lower edge being portion of said dielectric separation layer proximal to said substrate;

redistributing a dopant from said polycrystalline semiconductor plug into said substrate;

etching through any remaining film layers within a region substantially circumscribed by said dielectric boot to said topmost surface of said substrate; and

depositing an emitter polycrystalline semiconductor layer over said topmost surface of said substrate.

2. The method of claim 1 wherein said film stack is comprised of a first oxide layer, a first nitride layer, a first polysilicon layer, a second nitride layer, and an isolation oxide.

3. The method of claim 1 wherein the spacer is comprised of oxide.

4. The method of claim 1 wherein the spacer is comprised of polycrystalline silicon.

5. The method of claim 1 wherein the step of filling said slot region with said polycrystalline semiconductor plug material is achieved by depositing a conformal polycrystalline semiconductor plug material and anisotropically etching said polycrystalline semiconductor plug material prior to depositing a dielectric separation layer.

6. An electronic device comprising:

a semiconductor substrate having thereon at least one region laterally enclosed by a dielectric isolation region and coupled to a principal surface of said substrate;

a polycrystalline semiconductor plug region peripherally disposed on an outermost boundary of the dielectric region and coupled to said dielectric isolation region, said polycrystalline semiconductor plug region further being electrically coupled to said semiconductor substrate; and

a doped region extending from said polycrystalline semiconductor plug region distally into said substrate and electrically coupled to said polycrystalline semiconductor plug region, said doped region further having a doping concentration toroidal-like in topology.

7. The electronic device of claim 6 further comprising a polycrystalline semiconductor layer deposited within a region circumscribed by said dielectric isolation region.

8. The electronic device of claim 7 wherein the polycrystalline semiconductor layer is an emitter contact on a bipolar junction transistor.

9. The electronic device of claim 6 further comprising a second doped region peripherally bounded laterally by said doped region.

10. The electronic device of claim 6 wherein the doped region and the second doped region form a transistor base region.

11. A method of fabricating an electronic device comprising:

forming a slot region for a doped polycrystalline semiconductor plug material within an outer periphery of an etched window region, said wi ndow region formed by etching a film stack residing on a topmost surface of a substrate;

filling said slot region with said polycrystalline semiconductor plug material;

depositing a dielectric separation layer over said polycrystalline semiconductor plug and on an uppermost surface of said film stack;

depositing a spacer over said dielectric separation layer;

etching said spacer and said dielectric separation layer to form a dielectric boot shape on a lower edge of said dielectric separation layer, said lower edge being portion of said dielectric separation layer proximal to said substrate; and

redistributing a dopant from said polycrystalline semiconductor plug into said substrate.

12. The method of claim 11 wherein said redistributing results in a doping concentration toroidal-like in topology.

13. The method of claim 11 further comprising implanting a dopant into an area of said substrate located in a region circumscribed by said slot region.

14. The method of claim 11 further comprising etching through any remaining film layers within a region substantially circumscribed by said dielectric boot to said topmost surface of said substrate and depositing an emitter polycrystalline semiconductor layer over said topmost surface of said substrate.

15. The method of claim 11 wherein said film stack is comprised of a first oxide layer, a first nitride layer, a first polysilicon layer, a second nitride layer, and an isolation oxide.

16. The method of claim 11 wherein the spacer is comprised of oxide.

17. The method of claim 11 wherein the spacer is comprised of polycrystalline silicon.

18. The method of claim 11 wherein the step of filling said slot region with said polycrystalline semiconductor plug material is achieved by depositing a conformal polycrystalline semiconductor plug material and anisotropically etching said polycrystalline semiconductor plug material prior to depositing a dielectric separation layer.